

IMEC CORE CMOS

Boosting chip performance



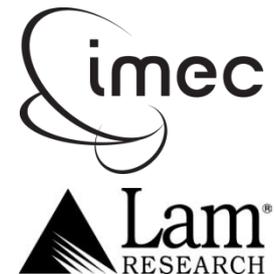


15NM HALF-PITCH PATTERNING: EUV + SELF-ALIGNED DOUBLE PATTERNING

IMEC CORE CMOS

JANKO VERSLUIJS, LAURENT SOURIAU, DAVID HELLIN*, ISABELLE ORAIN*, YOSHIE KIMURA*, EDDY KUNNEN, HAROLD DEKKERS, XIAOPING SHI, JOHAN ALBERT, VINCENT WIAUX, K Aidong XU

*IMEC, *LAM RESEARCH*



OUTLINE

Introduction

Litho Optimization

Application in 2 different integration stacks

- a-C stack
- a-Si stack

Summary & Conclusions

INTRODUCTION

15nm half pitch patterning is required for

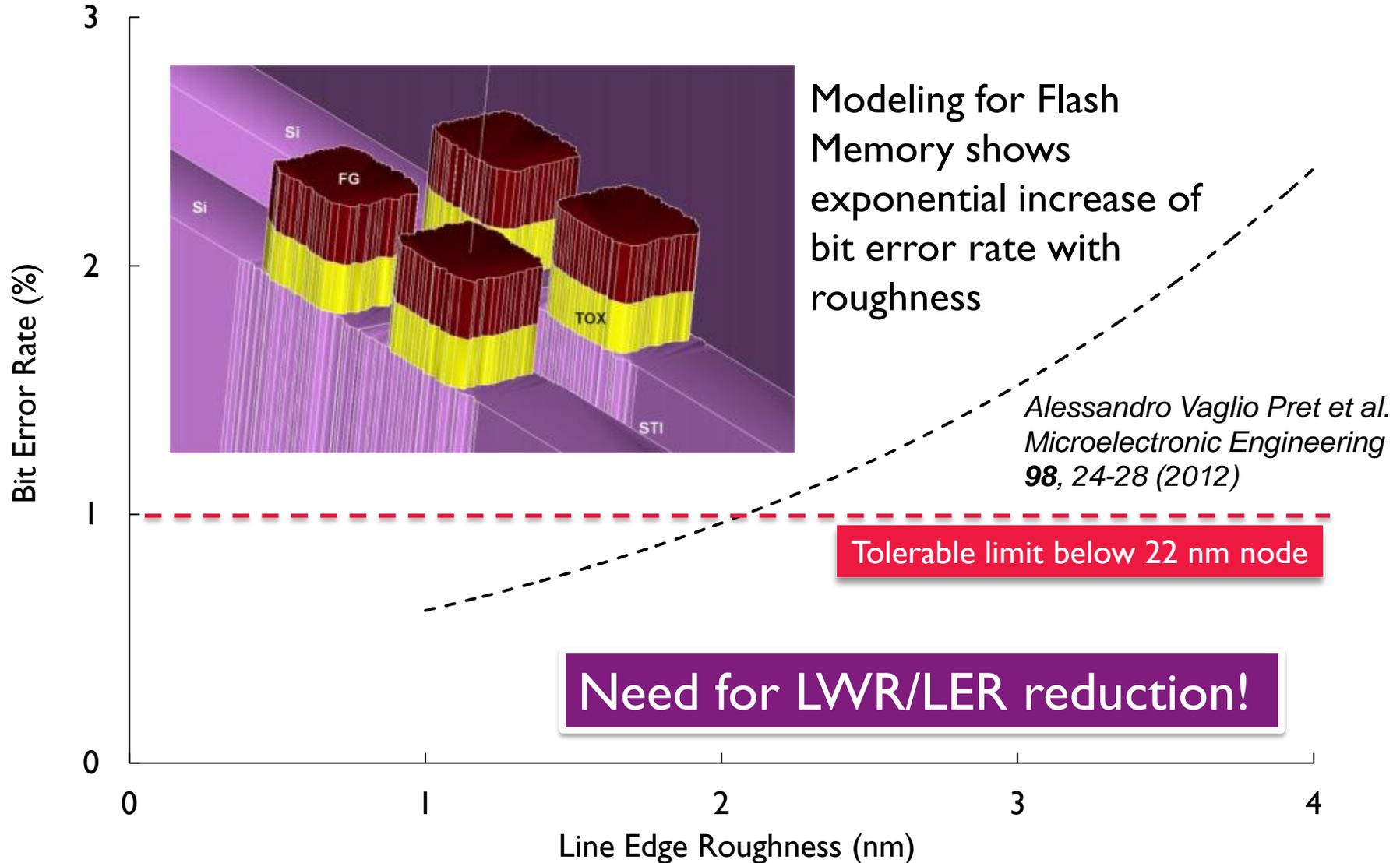
- 10nm Logic
- 15nm Floating Gate Flash memory applications

Several patterning options:

- Quadruple Patterning 193i
- Double Patterning EUV
- Single Patterning EUV
- DSA
-

Here we investigate **EUV + SADP** for 15hp

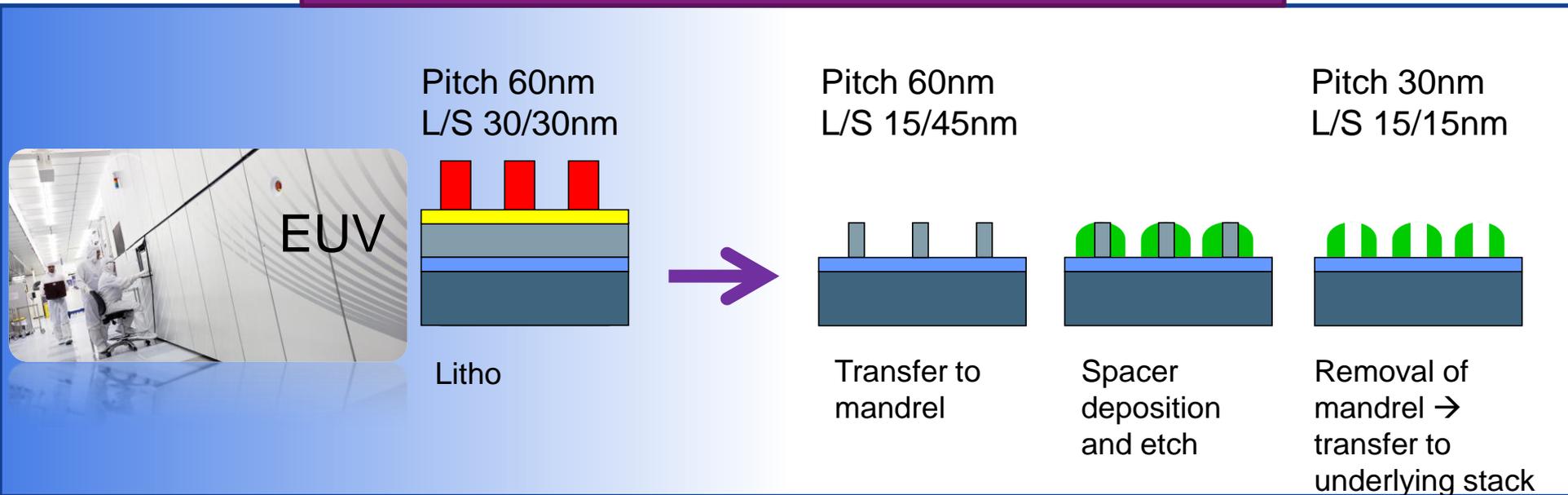
ROUGHNESS MODELING FOR ELECTRICAL FAILURE IN FLASH MEMORY



15NM HP PATTERNING

EUV+SADP

Schematic EUV+SADP patterning flow



OUTLINE

Introduction

 Litho Optimization

Application in 2 different integration flows

- a-C stack
- a-Si stack

Summary & Conclusions

TECHNICAL DETAILS

Litho:

ASML ADT & NXE 3100

Etch:

Lam Research 2300® Kryo® C Series conductor etch system

Target structures:

- Vertical 30nm L/S structures

Metrology: Hitachi CG4000_2

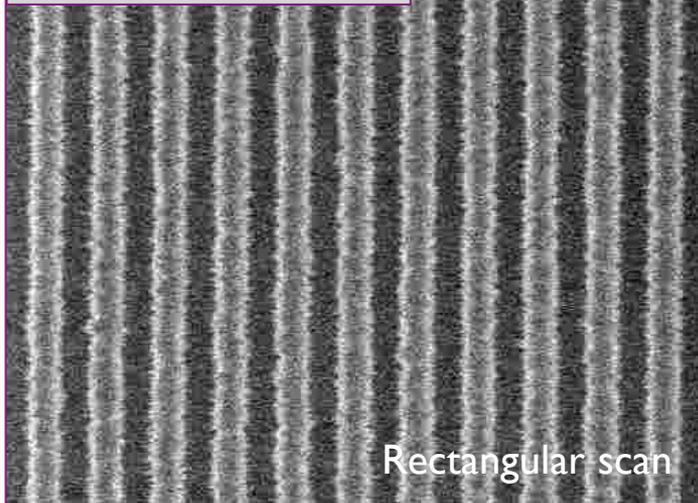
Litho: Beam: 500V, 8pA, HR

Etch: Beam: 800V, 8pA, HR

	CD	LWR
Magnification	300k	49k x 300k
Image	TV32	TV128
#lines measured	>3	>3
Measurement point	124	400
Sum lines	32	2
Inspect area	400	400
Smoothing	7	7
Threshold	70%	70%

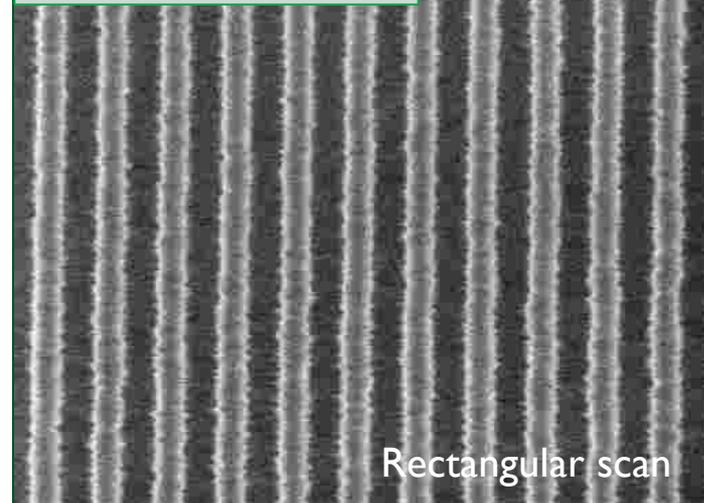
PROCESS TRANSFER TO NXE3100 AFTER LITHO

LWR=5.9nm
CD=30.5



ADT
TM07 reticle
Conventional
60nm SEVR140 / 20nm UL

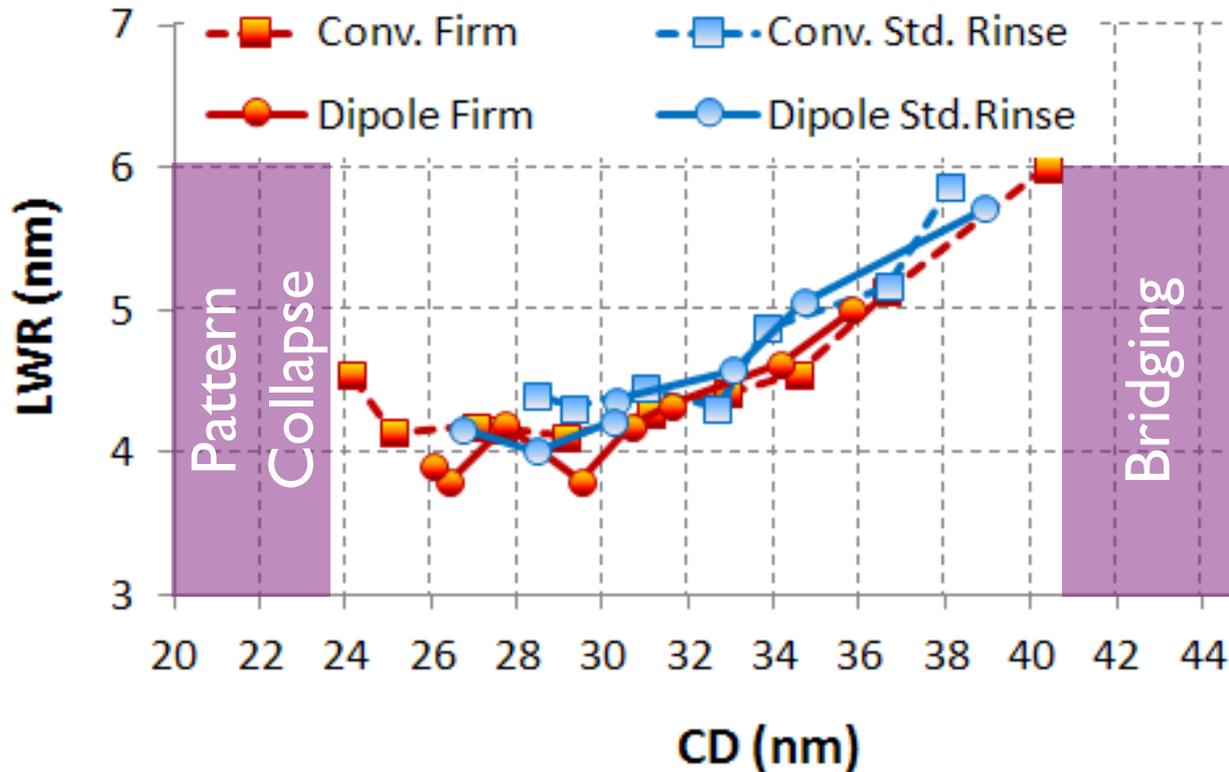
LWR=4.7nm
CD=30.8



NXE3100
RR14 reticle
Conventional
60nm SEVR140 / 20nm UL

LWR improvement ~ 1nm with new reticle + NXE

CONVENTIONAL VS. DIPOLE

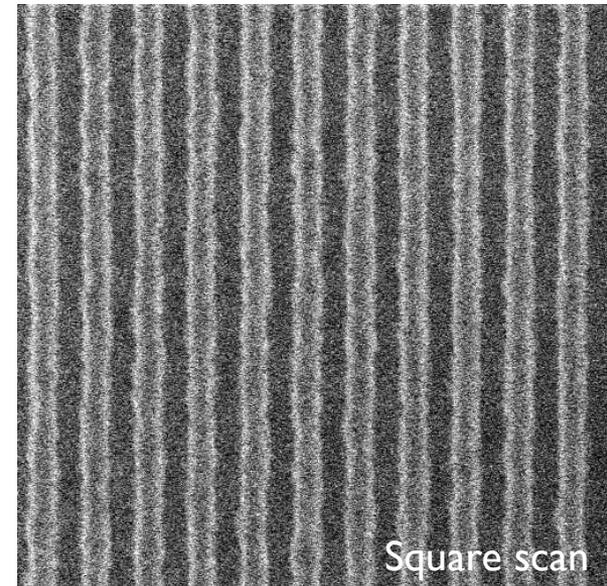
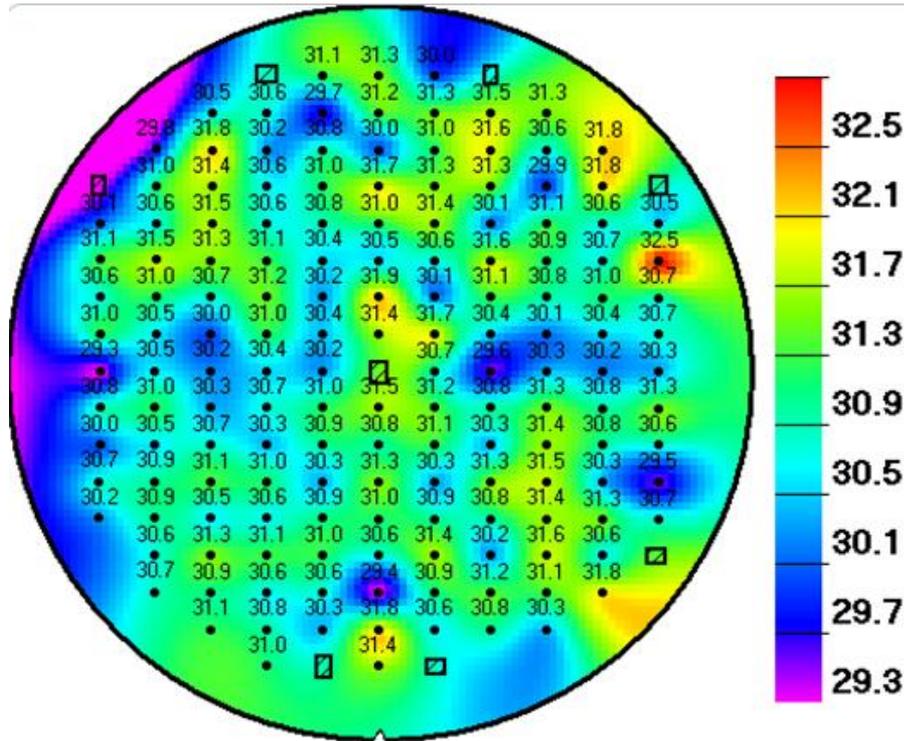


- LWR measured on FEM wafers through dose @ BF
- 16 measurements/die
- Measurement error ~0.3nm
- Pitch 60nm

- Target CD 30nm → no significant difference in LWR
- Selected conventional illumination – higher throughput

LITHO PROCESS OF RECORD

SEVRI40 – 60nm



- LWR = 4.7nm ; averaged over 25 die
- CD Mean = 30.8 nm at 30nm HP, CDU 3σ = 1.6nm

OUTLINE

Introduction

Litho Optimization

Application in 2 different integration flows



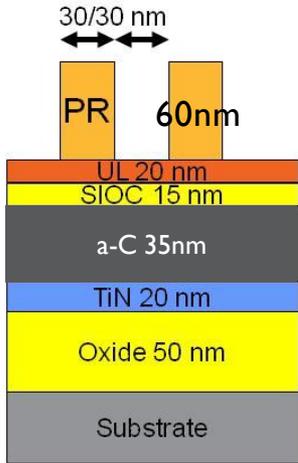
- a-C stack
- a-Si stack

Summary & Conclusions

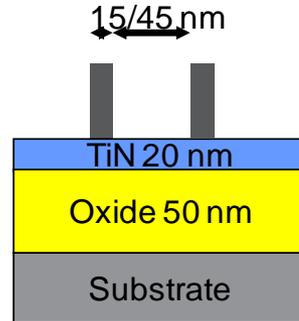
15NM HP PATTERNING

EUV+SADP

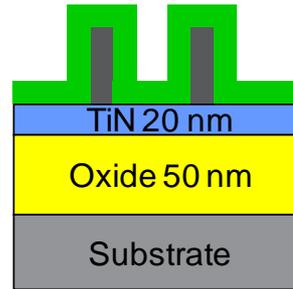
a-C stack for 15hp BEOL application



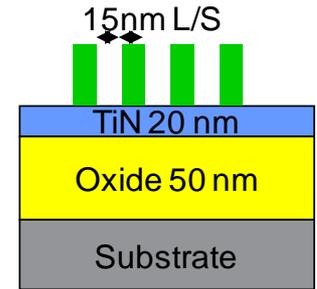
EUV litho



**Smoothing,
α-C stack etch
& SiOC removal**



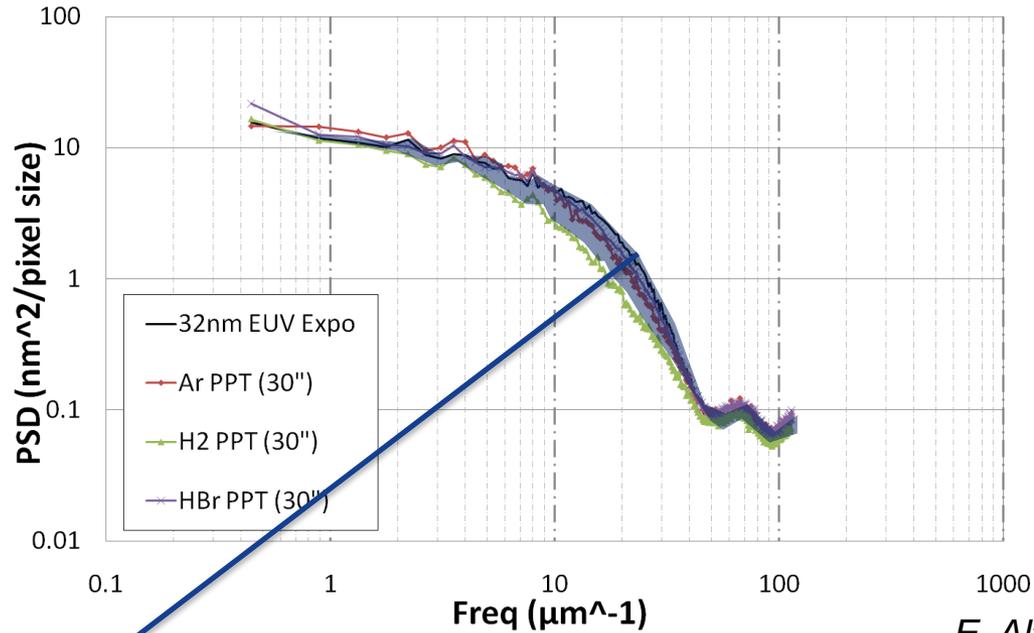
**SiN Spacer
deposition**



**Spacer etch
and α-C ash**

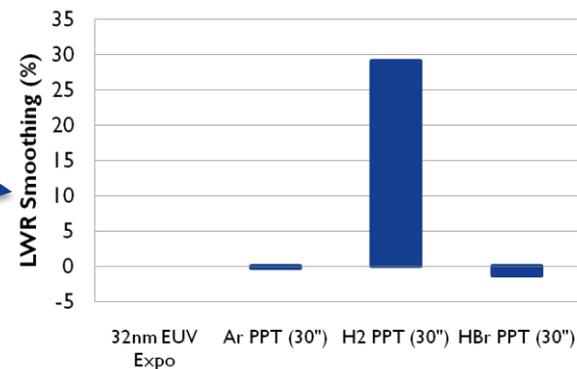
SMOOTHENING: PRE-PLASMA TREATMENTS ON A EUV PR H₂ PPT IMPROVES THE LER/LWR

□ Power Spectral Density (PSD) analysis done on 2.7 μ m length lines using 76 square scanned CDSEM images.

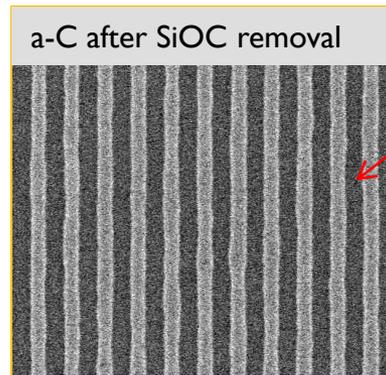
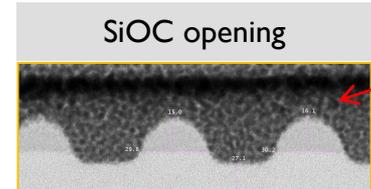
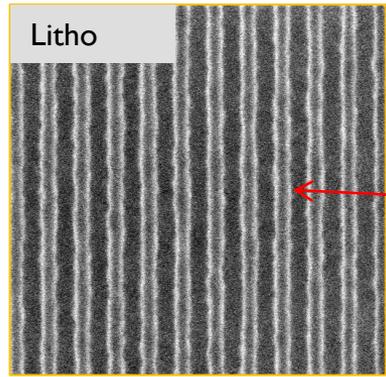


*E. Altamirano et al.
SPIE 2012, 83280L*

Any reduction on the area below the PSD is translated into a LER/LWR improvement.



RESIST to MANDREL Breakdown

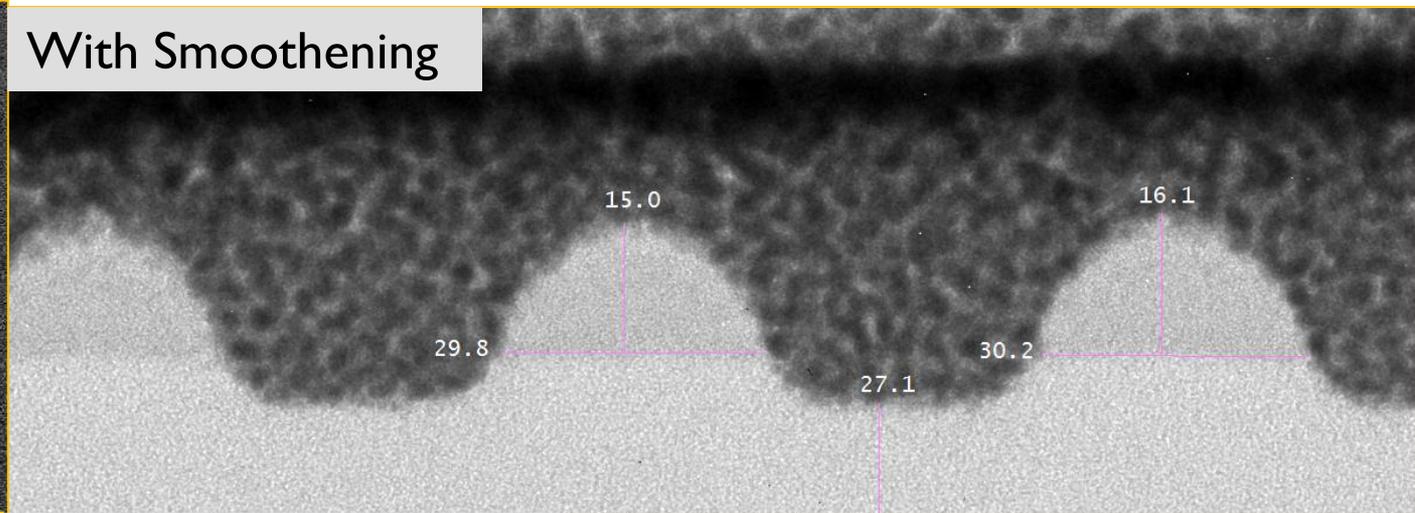


	CD (nm)	LWR (nm)	LWR σ (nm)	LER_left (nm)	LER_right (nm)
After litho	31.0	6.1	0.2	4.3	4.6
After hydrogen treatment	28.7	4.4	0.2	2.9	3.1
After encapsulation + UL open	28.3	4.2	0.2	2.9	3.0
After SiOC opening	28.9	6.1	0.3	3.4	3.9
After a-C etch	29.1	5.4	0.3	3.3	3.7
After SiOC removal	26.6	5.1	0.2	3.3	3.3

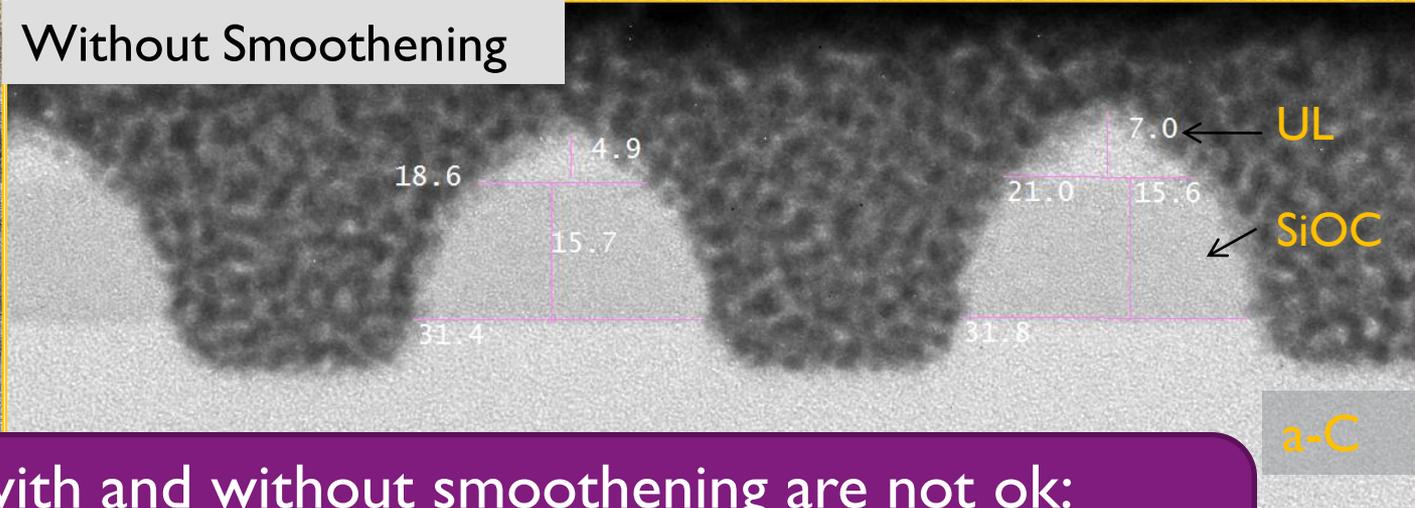
H2 PPT treatment smoothens resist lines, but LWR improvement is lost at the SiOC HM opening step

PROFILE AFTER SiOC OPENING STEP

With Smoothing

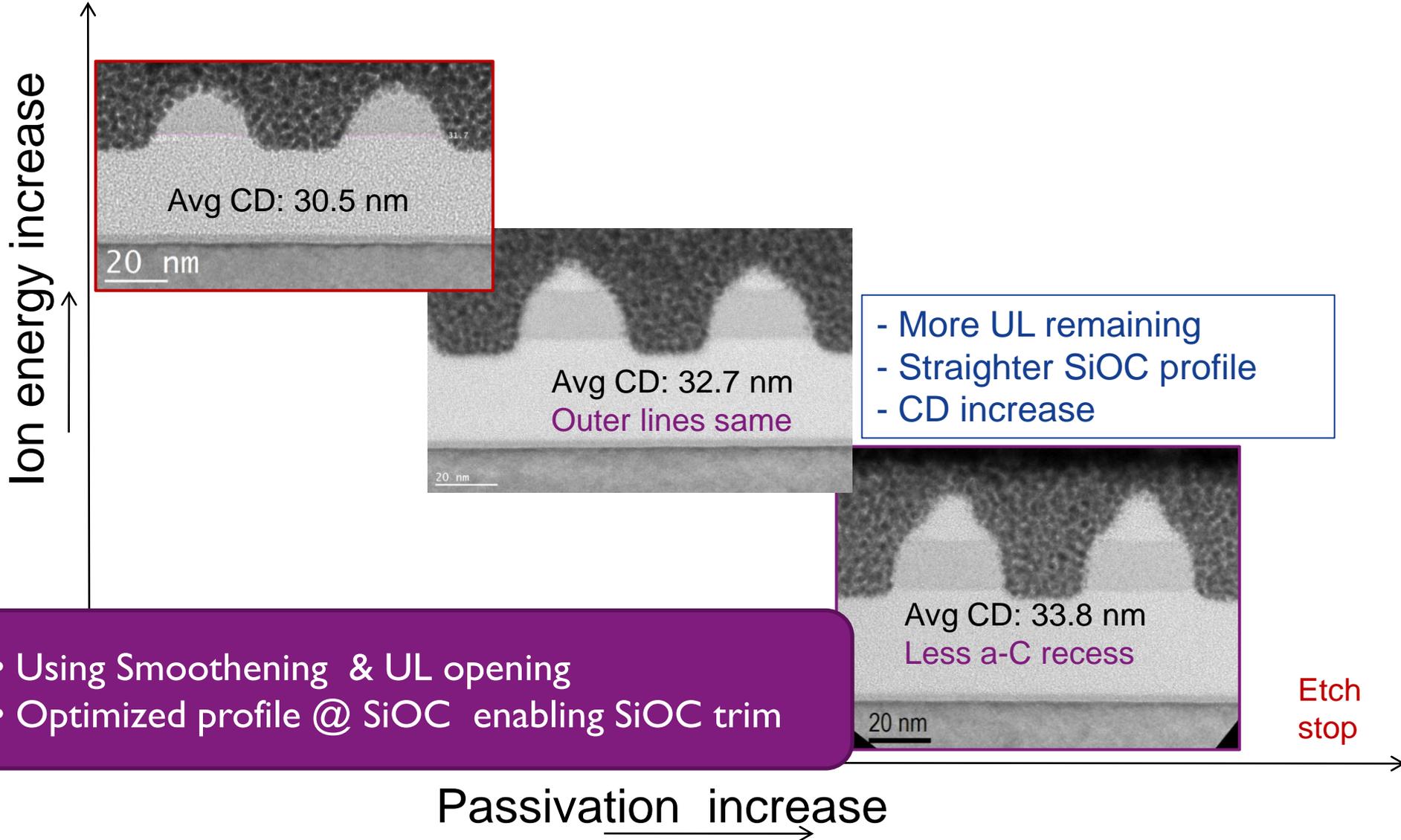


Without Smoothing



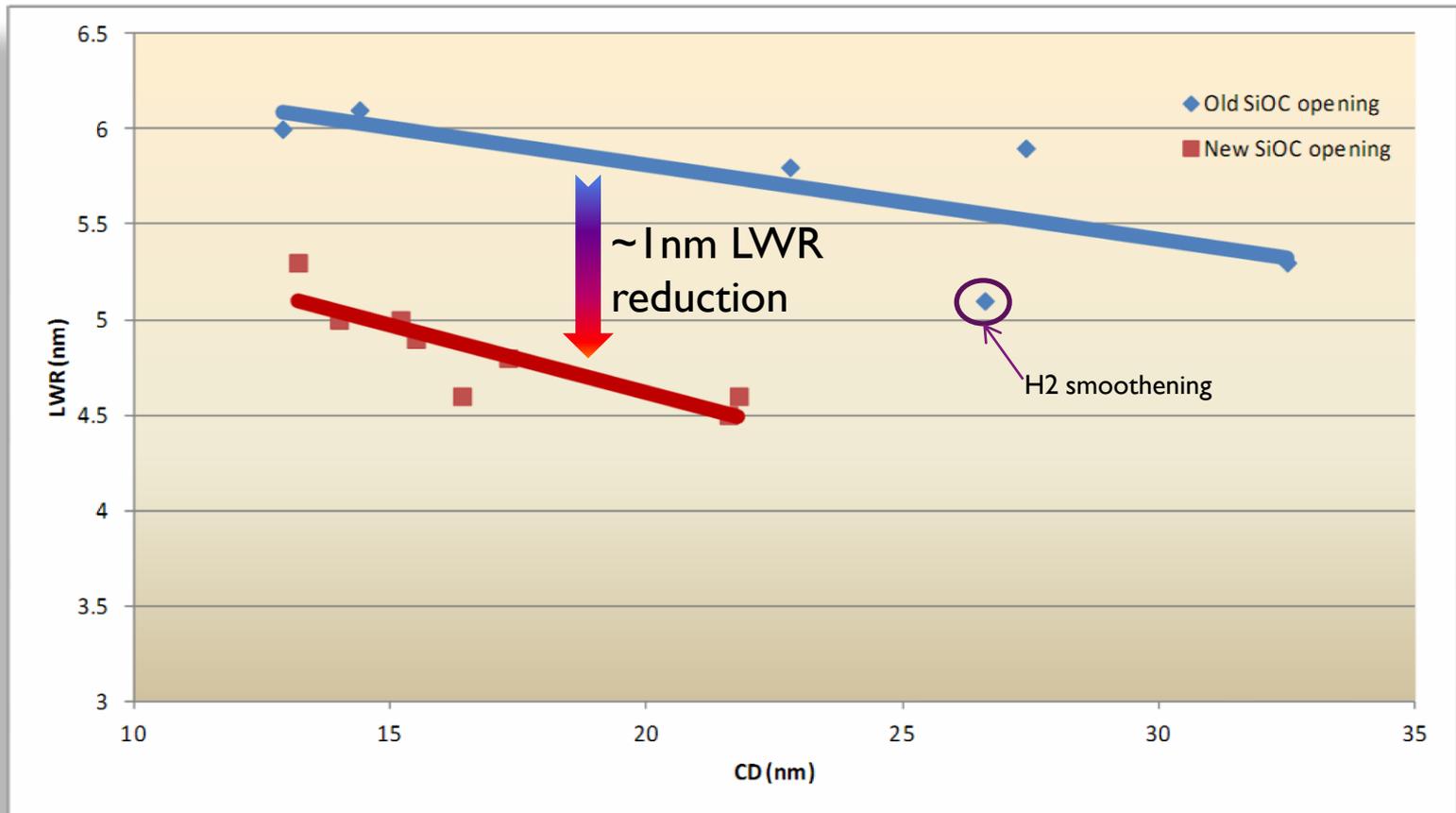
SiOC profiles with and without smoothing are not ok:
Not suitable for subsequent trim; increase of LWR
→ Need to improve SiOC opening etch step

SiOC OPENING OPTIMIZATION: EFFECT OF ION ENERGY AND PASSIVATION



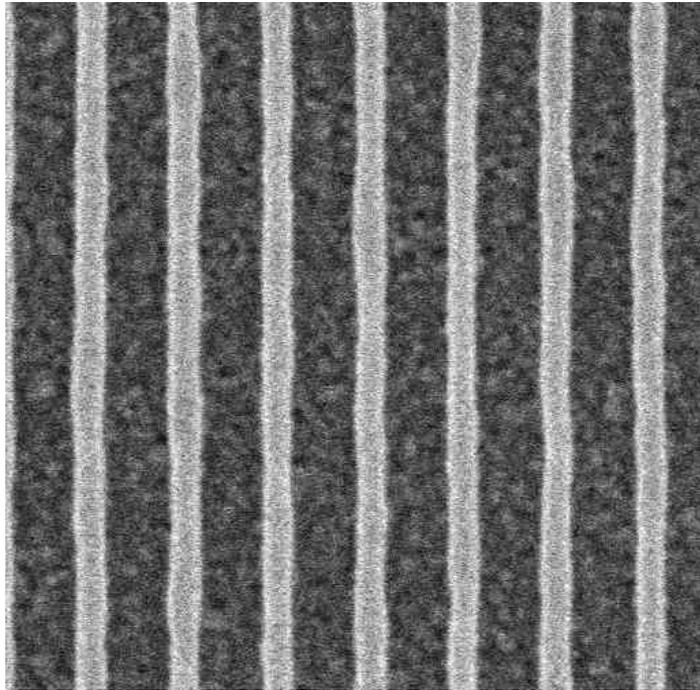
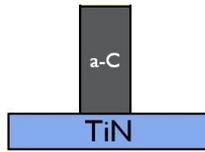
CD vs LWR

- AFTER SIOC REMOVAL



Optimized SiOC HM opening combined with trim gives improved mandrel LWR at target CD

FULL WAFER ETCH @ α -C MANDREL



				17.8	17.8	17.5				
		17.2	17.4	17.4	17.9	17.9	17.8	17.8		
	17.0	17.2	17.3	17.7	17.7	18.1	17.5	17.5	16.7	
	17.7	17.6	17.6	17.8	17.8	17.8	17.7	17.8	16.9	
17.3	17.2	17.7	18.0	18.3	18.0	18.0	17.8	17.8	17.4	17.1
17.1	17.3	17.7	18.3	18.5	18.2	18.1	18.1	17.5	17.2	17.4
17.2	17.4	17.6	17.8	18.0	18.3	18.3	18.3	18.1	17.3	16.9
17.7	17.2	17.8	18.5	18.6	18.4	18.3	18.4	18.0	17.1	17.3
17.4	17.3	17.8	18.1	18.1	18.2	18.5	18.2	18.2	17.4	17.2
16.9	17.3	17.6	18.1	18.4	18.2	18.4	18.0	18.1	17.6	17.3
17.2	17.3	17.5	18.4	18.0	18.3	18.3	17.9	17.8	17.4	17.2
17.3	17.1	17.2	17.8	17.9	18.5	18.2	17.9	17.7	17.2	17.4
16.8	17.0	17.4	17.2	18.0	17.9	17.7	17.7	17.5	17.2	17.3
	17.3	17.7	17.9	17.9	17.8	17.8	17.8	17.7	17.6	
	17.4	17.8	17.4	18.0	17.6	17.7	17.6	17.8	17.4	
		17.4	17.6	17.9	17.6	17.7	17.8	18.5		
			17.6	17.9	18.1	18.1	17.6			

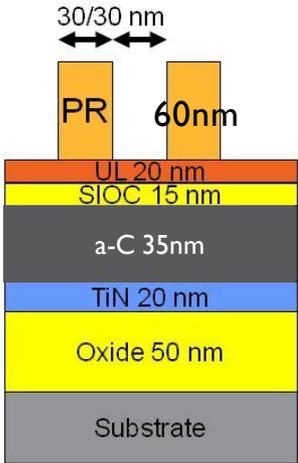
	CD	3σ_CD	LWR	σ_LWR	LER_left	LER_right
Litho	27.6	0.8	4.5	0.13	3.1	3.0
Mandrel patterning	17.7	1.2	4.1	0.16	2.8	2.8

Optimized HM opening results in improved LWR

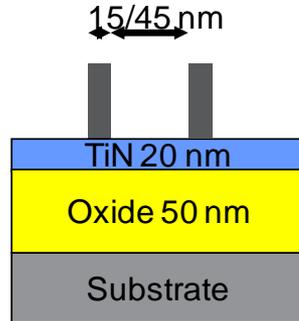
15NM HP PATTERNING

EUV+SADP

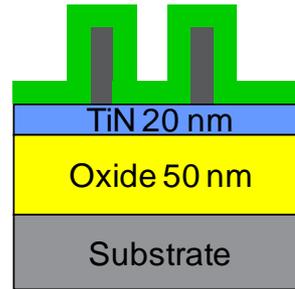
a-C stack for 15hp BEOL application



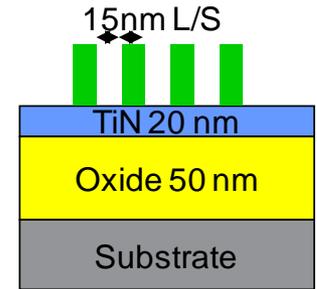
EUV litho



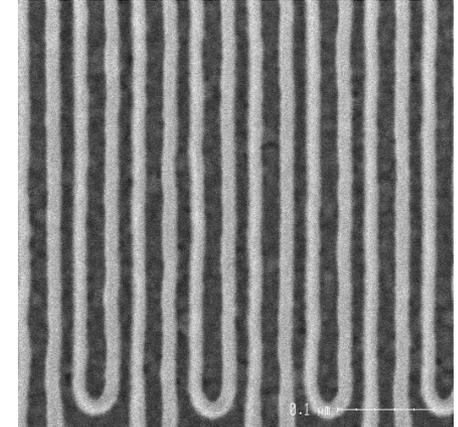
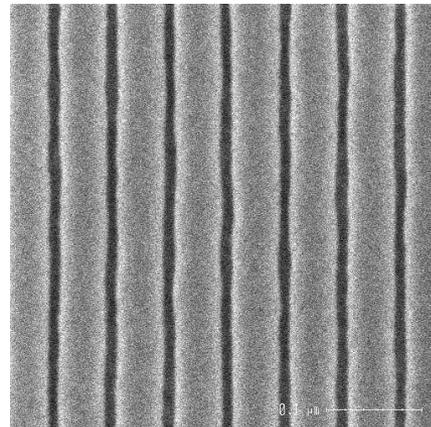
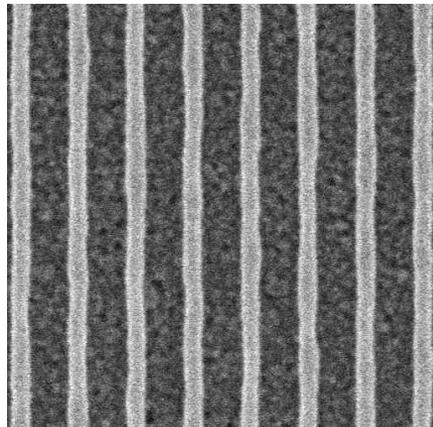
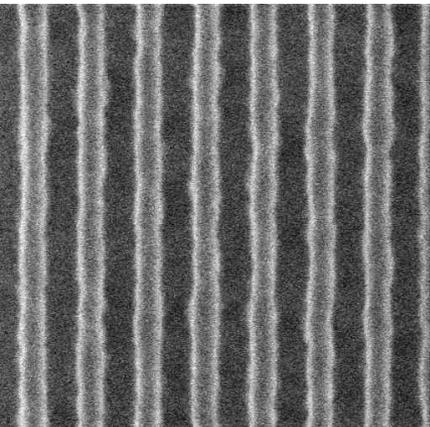
**α-C stack etch
& SiOC removal**



**SiN Spacer
deposition**



**Spacer etch
and α-C ash**



OUTLINE

Introduction

Litho Optimization

Application in 2 different integration flows

- a-C stack

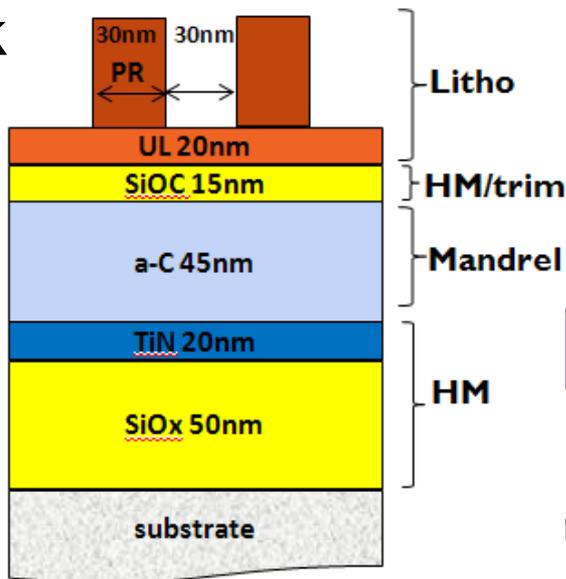


- a-Si stack

Summary & Conclusions

PATTERNING STACK MIGRATION

a-C stack

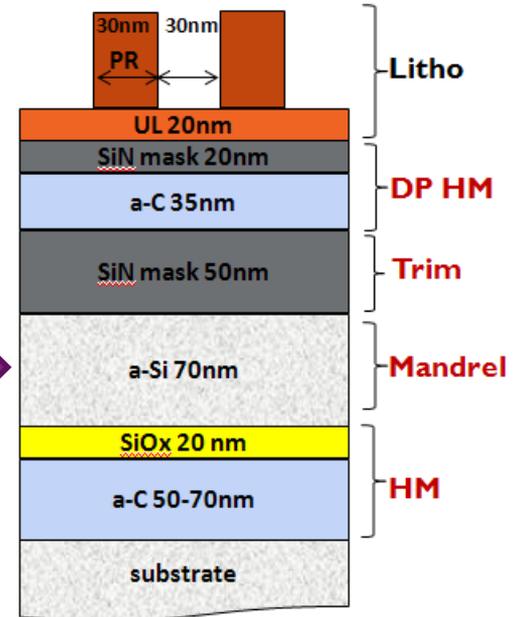


☹ Scalability

- SiOC mask is coupled with trim
- a-C mandrel: low Young's modulus → possible impact on line wiggling

- ☺ Low thermal budget compatible with BEOL applications

a-Si stack



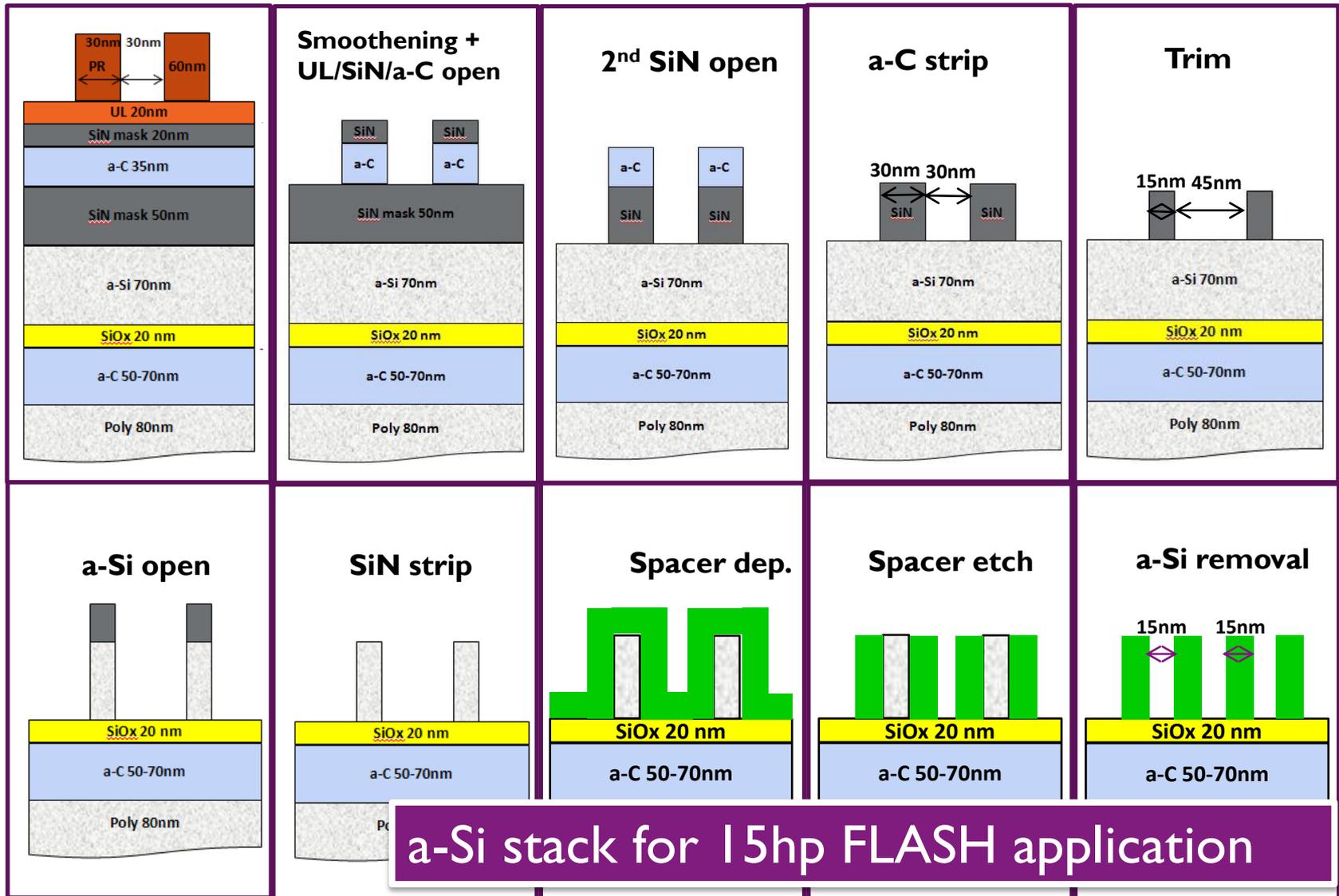
☺ Potential for lower LWR / scalability

- de-couple resist mask transfer (1st SiN/a-C & trim (2nd SiN/a-C))
- SiN mask instead of SiOC → LWR improvement
- a-Si mandrel: higher Young's modulus
- ☹ High thermal budget: issue with BEOL
- ☹ Complex stack/patterning

Stack migration

Targeting lower LWR/LER

a-SI STACK: PATTERNING FLOW



A-SI MANDREL PATTERNING: BREAKDOWN

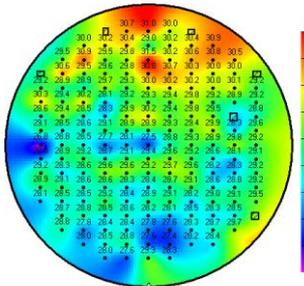
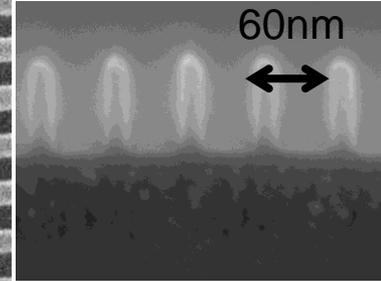
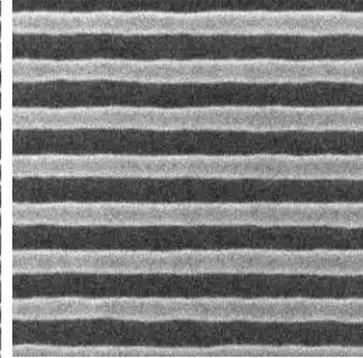
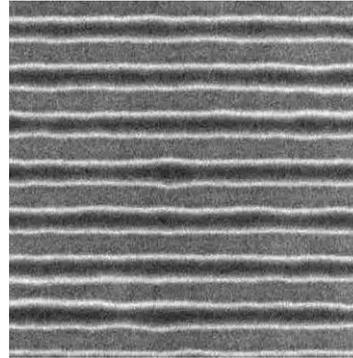
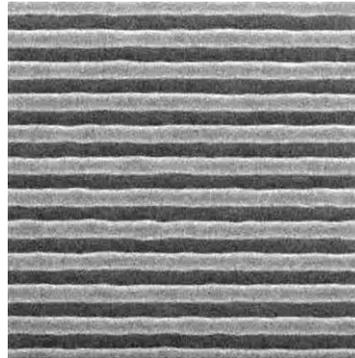
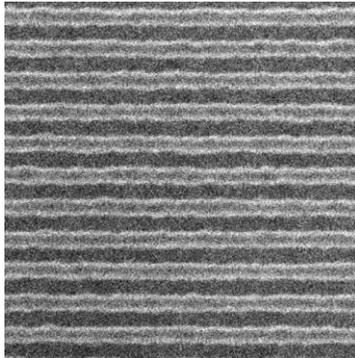
Litho

Smoothinging +
UL/SiN/a-C open

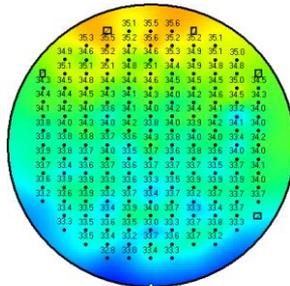
2nd SiN opening
+ a-C strip

a-Si opening

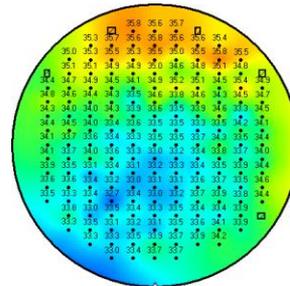
Center image



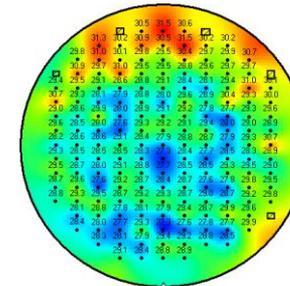
Mean : 29.1 nm
3-sigma: 2.6 nm (8.8 %)
Range : 4.7 nm (16.2 %)



Mean : 34.0 nm
3-sigma: 1.8 nm (5.4 %)
Range : 2.8 nm (8.2 %)



Mean : 34.1 nm
3-sigma: 2.4 nm (6.9 %)
Range : 3.2 nm (9.3 %)



Mean : 29.0 nm
3-sigma: 2.7 nm (9.4 %)
Range : 4.2 nm (14.5 %)

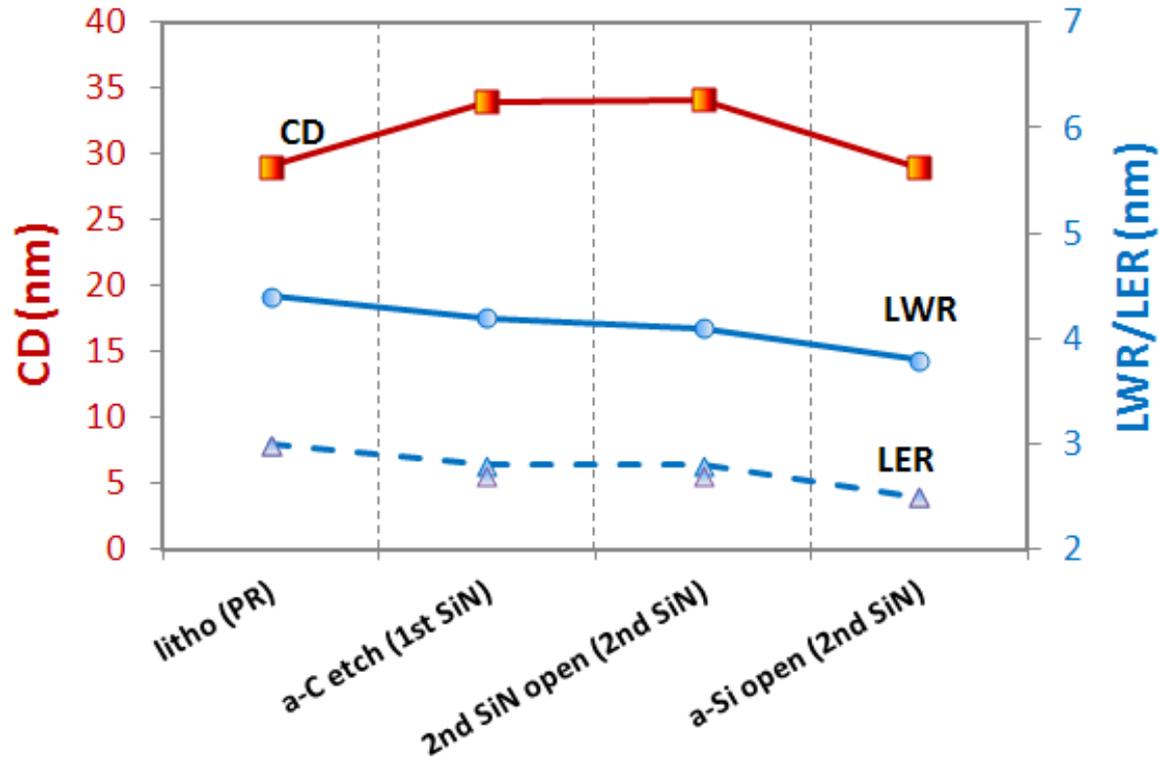
X-section SEM
a-Si mandrel after
wet SiN removal

Remark: litho CDU suffered
from within-wafer exposure
instability

After tuning plasma power,
gas and temperature
distribution

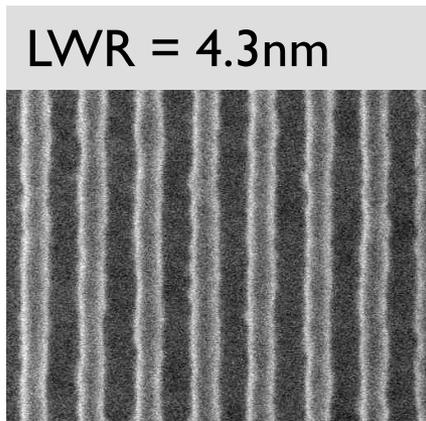
CD maintained from litho to a-Si opening at 29nm
CDU at ~2.7nm 3 σ level, optimized at etch, non-radial NU remaining

EVOLUTION OF CDU AND LWR

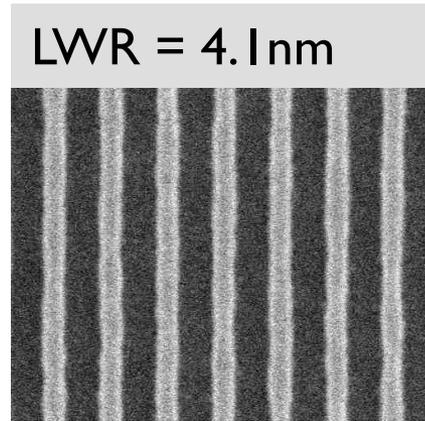


Post-litho CD maintained at 29nm after a-Si open
Mask open steps maintained LWR/LER as after litho
Small but systematic improvement of LWR through etch steps (0.6nm LWR)

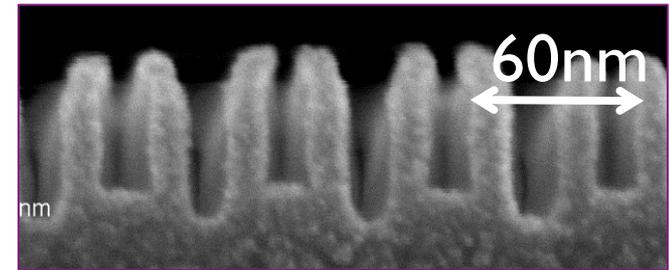
AFTER SPACER PATTERNING & AFTER SiOC ETCH



Litho



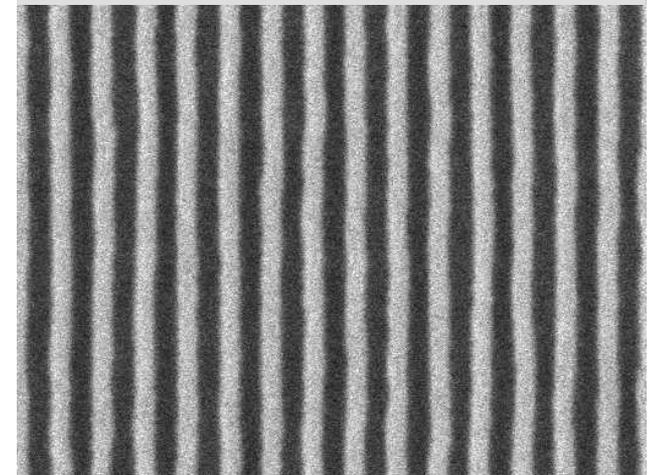
Mandrel Patterning +
SiN removal



Spacer Patterning



Core Gap LWR = 3.3nm
Spacer Gap LWR = 3.0nm



SiOC Opening

Post-litho LWR improved through etch steps:

- LWR = 4.3 \rightarrow 4.1nm

Spacer patterning & subsequent transfer into underlying SiOC layer gives

- Core Gap LWR = 3.0nm
- Spacer Gap LWR = 3.3nm

OUTLINE

Introduction

Litho Optimization

Application in 2 different integration flows

- a-C stack
- a-Si stack

 Conclusions

CONCLUSIONS

Self-Aligned Double Patterning is used in combination with EUV lithography to obtain 15nm HP structures

15hp EUV + SADP is applied in two different integration stacks

Process Optimization (litho, etch & trim) is needed to maintain or improve LWR/LER through the process flow

- After litho LWR = 4.5nm @ 30nm HP
- H₂ Plasma treatment can improve LWR
- HM opening and choice of HM material is crucial for LWR control
- After Spacer patterning and subsequent transfer into underlying stack
Core Gap LWR = 3.3nm @ 15nm HP



**ASPIRE
INVENT
ACHIEVE**

